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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/086,155
Filing Date	February 26, 2002
First Named Inventor	Masaaki KATOH
Art Unit	2811
Examiner Name	S. Hu
Total Number of Pages in This Submission: 14	Attorney Docket Number: 259052002900

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form + duplicate for fee processing (2 pages)
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)** (11 pages)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MORRISON & FOERSTER LLP (Customer No. 25226)		
Signature			
Printed name	Ilya Chorny		
Date	April 20, 2006	Reg. No.	56,519

Client Reference No.: SP3862US/TF

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV534443562US, in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: April 20, 2006 Signature: Georgina Matos (Georgina Matos)

pa-1061383

PTO/SB/17 (01-06)
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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	10/086,155
Filing Date	February 26, 2002
First Named Inventor	Masaaki KATOH
Examiner Name	S. Hu
Art Unit	2811
Attorney Docket No.	259052002900

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 03-1952 Deposit Account Name: Morrison & Foerster LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
5 - 20 =	0	x 50.00	= 0.00

HP = highest number of total claims paid for, if greater than 20.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
360.00	0.00

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
2 - 3 =	0	x 200.00	= 0.00

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50	_____ (round up to a whole number) x	250.00	= 0.00

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY					
Signature		Registration No. (Attorney/Agent)	56,519	Telephone	(650) 813-5932
Name (Print/Type)	Ilya Chorny			Date	April 20, 2006

Client Reference No.: SP3862US/TF

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV534443562US, in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: April 20, 2006 Signature: Georgina Matos (Georgina Matos)

Docket No.: 259052002900
Client Reference No.: SP3682US/TF

PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masaaki KATOH

Application No.: 10/086,155 Confirmation No.: 2654

Filed: February 26, 2002 Art Unit: 2811

For: LIGHT-EMITTING DIODE AND ITS MANUFACTURING METHOD Examiner: S. Hu

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is filed within 3 months of the Notice of Appeal filed in this case on January 20, 2006, and is in furtherance of said Notice of Appeal. The petition for a one month extension of time under 36 C.F.R. § 1.136 was filed with an amendment after the notice of appeal filed on April 19, 2006.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

SHARP KABUSHIKI KAISHA

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 5 claims pending in application.

B. Current Status of Claims

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: 11
3. Claims pending: 1, 8, 10, and 26
4. Claims allowed: none
5. Claims rejected: 1, 8, 10, and 26

C. Claims On Appeal

The claims on appeal are claims 1, 8, 10, and 26

IV. STATUS OF AMENDMENTS

Applicant filed an amendment after filing the notice of appeal on April 19, 2006. The amendment addressed the Examiner's objection in the final Office Action mailed on September 20, 2005. The Examiner has not acted on the amendment.

The claims in the Claims Appendix incorporate the amendments indicated in the amendment filed on April 19, 2006. No claims amendments have been made since that date.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claimed inventions are directed to a surface mounted light-emitting diode (LED). The light-emitting diode is comprised of a light-emitting diode chip mounted on a surface of a printed substrate (*see e.g.* page 3 lines 10-11; Figure 1).

The light-emitting chip comprises a transparent substrate (*see e.g.* page 9, lines 13-14; Figure 3 [**11**]), and a semi-conductor layer laminated on the substrate (*see e.g.* page 9, lines 11-12; Figure 3 [**12, 13, 14**]). The semiconductor layer comprises an N-type semiconductor layer and a P-type semiconductor layer, forming a PN junction at the interface between the P-type and N-type semiconductor layer (page 9, lines 11-12; Figure 3 [**12, 14**]). The semiconductor layer further includes a light-emitting portion in the vicinity of the PN junction interface (*see e.g.* page 9, line 12; Figure 3 [**13**]), and a first face and a second face, wherein both the first face and the second face are parallel to the transparent substrate, wherein the first face is in contact with the transparent substrate (*see e.g.* Figure 3 and Figure 4). The light-emitting chip further includes a pair of electrodes for applying voltage to the semiconductor layer (*see e.g.* page 9, lines 20-21, and pages 10, lines 2-3; Figure 3 [**5a, 5b**]), a light reflecting layer formed of a metal thin film formed on the second face of the semiconductor layer substantially parallel to the PN junction interface and for reflecting light emitted from the light-emitting portion (*see e.g.* page 9, lines 22-23; Figure 3 [**3**]), and a recessed section formed at a corner of the semiconductor layer. The recessed section is formed through the light reflecting layer and a portion of the semiconductor layer to form an exposed surface of one of the N-type semiconductor layer and the P-type semiconductor layer (*see e.g.* page 9, lines 16-19; Figure 3). One of the electrodes is formed on the light-reflecting layer (*see e.g.* page 10, lines 2-3;

Figure 3 [**5b**]) and the other electrode is formed on the exposed surface (*see e.g.* page 9, lines 19-21; Figure 3 [**5a**]).

The light-emitting chip is mounted on the printed substrate such that the PN junction interface is perpendicular to the surface of the printed substrate (*see e.g.* page 8, lines 10-13; Figure 1). In addition, the light-emitting chip is mounted such that the recessed section, having the exposed surface on which an electrode is formed, is adjacent to the printed substrate (*see e.g.* page 10, lines 13-15; Figure 1 [**5a, 5b**]),

Independent claim 1 is directed to a light-emitting diode comprising, "a light-emitting diode chip mounted on a surface of a printed substrate" (*see e.g.* page 3 lines 10-11; Figure 1). "The light-emitting diode chip including, a transparent substrate (*see e.g.* page 9, lines 13-14; Figure 3 [**11**]), a semiconductor layer laminated on the transparent substrate (*see e.g.* page 9, lines 11-12; Figure 3 [**12, 13, 14**], and formed of an N-type semiconductor layer and a P-type semiconductor layer" (page 9, lines 11-12; Figure 3 [**12, 14**]), "wherein a PN junction interface between the N-type and P-type semiconductor layers is perpendicular to the surface of the printed substrate" (*see e.g.* page 8, lines 10-13; Figure 1). The semiconductor layer includes, "a light-emitting portion in the vicinity of the PN junction interface (*see e.g.* page 9, line 12; Figure 3 [**13**]), and a first face and a second face, both the first face and the second face parallel to the transparent substrate wherein the first face is in contact with the transparent substrate" (*see e.g.* Figure 3 and Figure 4) "a pair of electrodes for applying voltage to the semiconductor layer (*see e.g.* page 9, lines 20-21, and pages 10, lines 2-3; Figure 3 [**5a, 5b**]), a light reflecting layer formed of a metal thin film formed on the second face of the semiconductor layer substantially parallel to the PN junction interface and for reflecting light emitted from the light-emitting portion (*see e.g.* page 9, lines 22-23; Figure 3 [**3**]), and a recessed section formed at a corner of the semiconductor layer adjacent to the printed substrate the recessed section formed through the light reflecting layer and a portion of the semiconductor layer to form an exposed surface of one of the N-type semiconductor layer and the P-type semiconductor layer" (*see e.g.* page 9, lines 16-19; Figure 3). "A first electrode of the pair of electrodes is formed on the light reflecting layer (*see e.g.* page 10, lines 2-3; Figure 3 [**5b**]), and a second electrode of the pair of

electrodes is formed on the exposed surface (*see e.g.* page 9, lines 19-21; Figure 3 [**5a**]), adjacent to the printed substrate (*see e.g.* page 10, lines 13-15; Figure 1 [**5a**])".

Claim 8, which depends from claim 1, recites that the metal thin film has a thickness of 100 nm or more (*see e.g.* page 5, lines 3-5).

Claim 10, which depends from claim 1, recites that the transparent substrate is transparent to color emitted by the light-emitting diode chip (*see e.g.* page 12, lines 5-8).

Claim 26, which depends from claim 8, which depends from claim 1, recites that the transparent substrate is transparent to color emitted by the light-emitting diode chip (*see e.g.* page 12, lines 5-8).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The Examiner objected to claims 1, 8, 10, and 26. The Examiner stated that in claim 1, "a recessed section formed through" needs further clarification, as it is not clear where such recess is form [sic], what it is formed of, and/or what is removed so as to form it" (Paper no. 20050916, page 2, third paragraph).

2. Claims 1, 8, 10 and 26 ("rejected claims") have been rejected under 35 U.S.C. 103(a) as allegedly being anticipated over U.S. Patent Application No. 2002/0117672 (the Chu et al. reference) in view of U.S. Patent No. 5,670,797 (the Okazaki reference) and/or U.S. Patent Application No. 2004/0051109 (the Ishizaki reference).

VII. ARGUMENT

1. Claim Objections

A. The Applicants traverse the Examiner's objection.

With respect to the first objection the limitation of claim 1 clearly states where the recessed section is formed, "**at the a corner** of the semiconductor layer", what is removed to form it "formed through the **light reflecting layer** and **a portion of the semiconductor layer** to form an exposed surface of one of the N-type semiconductor layer and the P-type semiconductor layer" (Emphasis added).

2. Rejection Under 35 U.S.C. 103(a)

A. The Examiner failed to prove a *prima facie* case of obviousness because neither the Chu et. al. reference, the Okazaki reference, nor the Ishizaki reference teach all the limitations of the rejected claims, for example, "a recessed section **formed at a corner** of the semiconductor layer ... to form an exposed surface of either the N-type or the P-type semiconductor layer". (Emphasis added.)

The Examiner states in his argument, with respect to the above-recited limitation, that the Chu et al. reference teaches "that the semiconductor layer has a recessed section at a corner of the semiconductor layer" limitation (Paper no. 20050916, page 3, second paragraph). The Chu et al. reference fails to teach a recessed section formed at a corner of a semiconductor layer. The recessed section as shown, for example, in Figs 1-6, of the Chu et al. reference, does not show a recessed section formed at a corner of the semiconductor layer. Figs. 1-6, show only a cross sectional view of the device taught by the Chu et al. reference. Accordingly, one of ordinary skill in the art would not conclude that the recessed section shown in Figs. 1-6 of the Chu et al. reference is formed at a corner of the semiconductor layer, as recited in the rejected claims.

The Okazaki reference, fails to cure this deficiency because it does not teach a semiconductor layer having a recessed section, much less, a recessed section at a corner of the semiconductor layer.

Additionally, the Ishizaki reference fails to cure this deficiency because, like the Chu et al. reference, the Ishizaki reference fails to teach a recessed section formed at a corner of a semiconductor layer and shows only a cross sectional view of the device taught by the Ishizaki reference, as shown for example in Fig. 6. Accordingly, one of ordinary skill in the art would not conclude that the recessed section, shown in Fig. 6, of the Ishizaki reference is formed at a corner of the semiconductor layer, as recited in the rejected claims.

In light of the above arguments, the Chu et. al. reference, the Okazaki reference, and the Ishizaki reference individually or in combination fail to teach all of the limitations of the rejected claims and thus the rejection under 35 U.S.C. 103(a) should be withdrawn and the claims should be allowed to issue.

B. The Examiner failed to prove a *prima facie* case of obviousness because there is not sufficient motivation to combine the teachings of the Chu et al. reference and with the Okazaki reference.

In the LED disclosed in the Okazaki reference, the light is emitted parallel to the PN junction surface. In contrast, in the LED disclosed in the Chu reference, the light is emitted vertical to the PN junction surface. Therefore the structure of the LED's in the Okazaki and the Chu et al. references are different. Thus, it would not be obvious to one of ordinary skill in the art to combine the teaching of the Okazaki reference with the teachings of the Chu et al. reference without any suggestion or motivation to do so.

Further, the Chu et al. reference teaches away from using the mounting structure as taught in the Okazaki reference. In the LED, shown in Fig. 1B of the Chu et al. reference, the electrodes are on one side of the semiconductor layer and the light is emitted on the **side opposite**

the electrodes through the transparent substrate 107. The electrodes contain mounting bumps 112 and 113 used to mount the LED to the substrate such that "both the P-electrode and the N-electrode **face downwardly** so that the blue light created is projected out ..." (*see e.g.* Chu et al., col. 1, paragraph [0009]). (Emphasis added). Thus, the device, in Fig. 1B of the Chu et al. reference, is configured so that light is emitted upwardly, **perpendicular to the surface of the substrate** to which it is mounted. If the mounting structure taught in the Okazaki reference is employed then electrode 110 and 111 in Fig. 1B would be placed sideways, and the light emitted through the transparent substrate would proceed in a horizontal direction, **parallel to the surface of the substrate**. Consequently, if the mounting structure as taught by the Okazaki reference is utilized **the direction of the emitted light is changed**. The direction of the emitted light is an essential property of LEDs, and the change of the direction of the emitted light would destroy the purpose of Chu et al.'s invention. Accordingly, one of ordinary skill in the art would not employ the mounting structure disclosed in the Okazaki reference with the LED disclosed in the Chu et al. reference. Thus, the rejection under 35 U.S.C. 103(a) should be withdrawn and the claims should be allowed to issue.

VIII. CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/086,155 (status as of June 30, 2005)

Claim 1: (previously presented) A light-emitting diode comprising a light-emitting diode chip mounted on a surface of a printed substrate, the light-emitting diode chip including:

a transparent substrate;

a semiconductor layer laminated on the transparent substrate and formed of an N-type semiconductor layer and a P-type semiconductor layer, wherein a PN junction interface between the N-type and P-type semiconductor layers is perpendicular to the surface of the printed substrate, the semiconductor layer including:

a light-emitting portion in the vicinity of the PN junction interface; and

a first face and a second face, both the first face and the second face parallel to the transparent substrate wherein the first face is in contact with the transparent substrate;

a pair of electrodes for applying voltage to the semiconductor layer;

a light reflecting layer formed of a metal thin film formed on the second face of the semiconductor layer substantially parallel to the PN junction interface and for reflecting light emitted from the light-emitting portion; and

a recessed section formed at a corner of the semiconductor layer adjacent to the printed substrate the recessed section formed through the light reflecting layer and a portion of the semiconductor layer to form an exposed surface of one of the N-type semiconductor layer and the P-type semiconductor layer;

wherein a first electrode of the pair of electrodes is formed on the light reflecting layer and a second electrode of the pair of electrodes is formed on the exposed surface adjacent to the printed substrate.

Claim 2-7 (cancelled)

Claim 8 (previously presented): A light-emitting diode claimed in Claim 1, wherein the metal thin film has a thickness of 100 nm or more.

Claim 9 (cancelled)

Claim 10 (previously presented): A light-emitting diode claimed in Claim 1, wherein the transparent substrate is transparent to color emitted by the light-emitting diode chip.

Claim 11 (withdrawn): A method for manufacturing a light-emitting diode comprising mounting, on a surface of a printed substrate, a light-emitting diode chip having a

substrate, a semiconductor layer which is laminated on a surface of the substrate, is formed of an N-type semiconductor layer and a P-type semiconductor layer and has a light-emitting portion in the vicinity of a PN junction surface between the N-type and P-type semiconductor layers, a pair of electrodes for applying voltage to the semiconductor layer, and a light reflection layer reflecting light emitted from the light-emitting portion, thereby obtaining the light-emitting diode, the method comprising, for mounting the light-emitting diode chip on the printed substrate,

the step of forming beforehand the light reflecting layer on a front surface or a back surface of the substrate of the light-emitting diode chip or in the light-emitting diode chip in such a manner that the light reflecting layer is approximately parallel to the PN junction surface, and

the step of fixing the obtained light-emitting diode chip on the printed substrate so that the PN junction surface is perpendicular to the surface of the spring substrate and electrically connecting the pair of electrodes of the light-emitting diode chip to the printed substrate.

Claim 12 -25 (cancelled)

Claim 26 (previously presented): A light-emitting diode claimed in Claim 8, wherein the transparent substrate is transparent to color emitted by the light-emitting diode chip.

Claim 27 (cancelled)

IX. EVIDENCE APPENDIX

This Appendix contains the following items, which were entered into record as described.

A. Chu et al. "High-Brightness Blue-Light Emitting Crystalline Structure" (U.S. Patent Publication No. 2002/0117672). This patent application publication was cited by the Examiner as part of a final rejection made in September 20, 2005.

B. Okazaki "Compact Light-Emitting Device With Sealing Member And Light-Transmitting Resin Seal" (U.S. Patent No. 5,670,797). This patent was cited by the Examiner as part of a final rejection made in September 20, 2005.

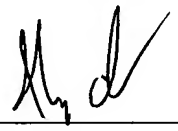
C. Ishizaki et al. "Light-Emitting Device And Its Manufacturing Method And Visible Light Emitting Device" (U.S. Patent Publication No. 2004/0051109). This patent application publication was cited by the Examiner as part of a final rejection made in September 20, 2005.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: April 20, 2006

Respectfully submitted,

By 

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